

## COMMUNICATIONS: High Speed Networks

Model #	Standards Supported	VCO Mhz	VCO Int/Ext	Tracking Range MBPS Min Max	Static Phase Error 2^7/°23-1 PRNS °25C Tmax	Received Clock Skew nsec Min Max	No Data Run Bit Periods	Output Jitter ρ=I 2^7/°23-1 PRNS Max	Jitter Tolerance Unit Intervals PP	Acq Time ρ=1/2 ζ=5	t rise max nsec	t fall max nsec	Vcc Volts	Icc mA
NON REGENERATION APPLICATIONS														
AD800-45	DS-3	44.736	Int	43 45.5	10° 11.5°	0.2 1	240	4.7° RMS	6.5 @2.3KHz .47 @30KHz .47 @1MHz	↓ ↓ ↓	1.5	1.5	-5.2V	205
AD800-25	STS-1	51.84	Int	49 53	↓ ↓	↓ ↓	↓ ↓	↓ ↓	830 @30Hz 7.4 @2KHz .47 @20KHz	↓ ↓ ↓	↓ ↓ ↓	↓ ↓ ↓	↓ ↓ ↓	↓ ↓ ↓
AD800-155	STS-3 STM-1	155.52	Int	155 156	30° 37°	↓ ↓	↓ ↓	↓ ↓	9.7° RMS 2 @6.5KHz .26 @26KHz	↓ ↓ ↓	↓ ↓ ↓	↓ ↓ ↓	↓ ↓ ↓	↓ ↓ ↓
REGENERATION APPLICATIONS														
AD803	PON's	20.48	Int	19.1 20.5	30° typ	1.95 13.6	1000	5.8° RMS	795 @10Hz 7.95 @1KHz .95 @10KHz	3*10^5	18.2	8.6		
AD805	G.958 TYPE A or B AD807 w/ ON CHIP QUANTIZER	155.52	Ext	± 7.7KHz	33° 33°	0.2 1.1	500	1° RMS	125 @30Hz 2.2 @6.5KHz .65 @1MHz	44	1.5	1.5	+5 or -5.2V	95
AD807	G.958 TYPE A	155.52	Int	155 156	20° 20°		NS	2.7° RMS	4.5 @6.5KHz .45 @65KHz .45 @1MHz	8*10^5	NS	1.5	+5V	37
AD808	OC-12, SDH STM-4	622	Int											
FREQUENCY SYNTHESIZER, 9.72 or 19.44MHZ INPUT														
AD809	SDH SONET	155.52		9.719 9.721				2.4° RMS typ		↓	NS	1.5	+5V	28
AD809	SDH SONET	155.52		19.438 19.442				↓						
UTP Category 5, or FTM 175M Cable														
				Frequency Synthesizer Input Output	Oscillator Circuit Center Freq	Clock Recovery PLL 2^23-11 nput		Output Jitter °			t rise max nsec	t fall max nsec	Vcc Volts	Icc mA
				Freq MHz	Freq MHz	Freq MHz	Deviation ppm	Jitter ° rms	Phase °	B'width KHz				
AD6816				9.72 or 19.44	155.52	19.44	82	3.5	20	100		2.1	2.1	+5 95
Fast Ethernet 100 Base TX Transceiver														
	<<<<<<<<<Receiver>>>>>>>>>	<<<<Signal Detect>>	Transmitter Line Driver											
	No Equalizer	Rise/Fall Time	Trip Level	Release Level	Rise/Fall Time	Output Jitter	Output Current Levels		Vcc	Icc				
	Data Run	Constant												
	Bit Periods	msec	nsec	mV min	mV min	nsec	psec	mA	Volts	mA				
ADM5104	100	1000	1	200	1000	3 typ	750 typ	0/20/40	5	320				
ADSL														
AD20MSP910	ADSL CHIPSET, AD6435 modem interface, AD6436 DMT Co-Processor, AD6437 Analog Front End, AD816 Line Driver and Receiver, ADSP2183 Fixed Point DSP													
Chip Sets														
MODEL NUMBER	Description													
IS54/IS136	IF BASEBAND CONVERSION, AD7011+AD7013+AD607													
AD6400	BASE BAND + RADIO CIRCUITRY FOR DECT: AD7011, AD7013, AD607 (GLOSSY)													
AD6600/6620	DIVERSITY BASE STATION RECEIVER, FOR NEW AIR STANDARDS (GLOSSY)													
AD6600	11 BIT, 8 BIT MANTISSA, 3 BIT EXPONENT, 20MSPS, INPUT CAN TRACT 200MHz Signal, DUAL CHANNEL., (D/Range=92dB 30dB Variable Atten.+62dB A/D GAIN RANGING & RSSI, for NARROW BAND APPL.													
AD6620	DUAL CHANNEL DECIMATING RECEIVER, 65MHz I or Q, 32.5MHz I&Q, w/COMPLEX NCO, QUADRATURE MIXER, 2 PRGM DECIMATION STAGES													
AD6640/6620	MULTI-CHANNEL/MULTI-MODE BASE STATION RECEIVER, FOR NEW AIR STANDARDS (GLOSSY)													
AD6640	12 BIT, 65MSPS, SFDR=80dB @ 30MHz,DIFF INPUT., +5V @ 90mA, TTL/CMOS output levels, Pins with AD9042 Except for Voffset Pin													
AD6620	DUAL CHANNEL DECIMATING RECEIVER, 65MHz I or Q, 32.5MHz I&Q, w/COMPLEX NCO, QUADRATURE MIXER, 2 PRGM DECIMATION STAGES													
AD20MSP410	GSM BASEBAND PROCESSING CHIPSET: ALG (Algorithm signal Processor=ASCIC Variant of ADSP2176 & ADSP2178, AD-PLP01, Physically Layer Processor=ASCIC +H8300H u/CONTROLLER, BBC, Base Band Converter=AD53/009-9 (AD													
AD20MSP415	GSM BASEBAND PROCESSING CHIPSET: AD6421+AD6422, COMES WITH LAYER S/WARE, ALSO AVAILAE OBJECT CODE & LICENSE FOR LAYERS 2&3 OF THE PROCOTOL STACK and USER INTERFACE DEVELOPMENT SYST													
	AD6421	GSM/DSC1800/PCS1900 VOICE BAND and BASEBAND CODEC, LAYER 1 PROCESSING OF GSM AIR INTERFACE, ENCLUDES OP-AMPS, FILTERS, A/D & D/A FOR VOICE,BASEBAND, AGC/AFC CONTROL & POWER												
	AD6422	GSM PROCESSOR, ADSP2181 + uCONTROLLER + 16 BIT CODEC, PART OF AD20MSP415 CHIP SET												